SystemX: HIEA

HETEROGENEOUS INTEGRATION OF EVERYTHING ONTO ANYTHING


Computing Is Everywhere

(not just here)
Heterogeneous Integration is Driving Research

- Societal “pull”: every day 2.5 exabytes are created

  “... a single advanced brain laboratory would produce 3 petabytes of data annually, roughly as much data as the world’s largest and most complex science projects [Large Hadron Collider (LHC)].”
  - Kavli Foundation (2013)

- Existing hardware not fast enough, consumes too much energy
- Companies often do not have the breadth to tackle full range from nanomaterials to systems

- Approaches:
  - In-memory computing
  - Monolithic 3D interleaving of memory & logic
  - Address dense-system thermal challenges
  - Process data in energy-efficient way at the source
  - Integrated sensors

HIEA Focus Area Vision

- Heterogeneous Integration of Everything onto Anything (HIEA)
- Integration of “beyond-Si” platforms for “beyond Moore” applications
  - Monolithic integration of logic, memory, sensors, thermal management, flexible substrates
  - Energy-efficient and brain-inspired design opportunities
  - Autonomous electronics and energy-harvesting opportunities

Example: Device Scaling Challenges

Gate Pitch is key metric of device scaling
Must scale both $L_G$ and $L_C$
May be possible ONLY with atomically thin channels

Project Areas and Topics

- Mid- & near-field wireless power with stretchable electronics (Fan)
- Chip-integrated thermoelectric power for wireless sensor networks (Goodson)
- Body-Heat-Powered Autonomous Wearable Electronics (Pop)
- Autonomous wireless sensor nodes for harsh environments via AlGaN/GaN heterostructures (Senesky)
Project Areas and Topics: 3D Monolithic Integration

- **Monolithic 3D integration** of logic & memory for energy-efficient computation (Mitra, Wong)
- Architectural studies of monolithic 3D integration benefits for energy-efficient computation (Mitra)
- Applications of Ge and III-Vs on Si for MOSFETs, photonics and photovoltaics (Saraswat)
- Fully integrated Thermal Management of 2D/3D Chips (Goodson)
- Electronic synaptic devices for brain-inspired computing (Wong)
- Integration of Atomically Thin 2D with 3D Materials and Devices (Pop)
- Transfer Printing Methods for Integrating Thin Film Electronics onto Any Substrates (Zheng)
- Autonomous wireless sensor nodes for harsh environments via AlGaN/GaN heterostructures (Senesky)
- Skin-like electrodes for long-term electrophysiological monitoring (Fan)
- Integration of local ILVs, no TSVs process T < 250 °C
- Applications of Ge and III-Vs on Si for MOSFETs, photonics and photovoltaics (Saraswat)
- X-on-Si
- X-on-flex
- Monolithic 3D Integration (Wong, Mitra)

**3D RRAM**
- Main memory, storage

**1D/2D FETs**
- ALU & flip-flops, register files, cache(L1)

**STTRAM**
- Cache (L2, L3), main memory

**1D/2D FETs**
- On-chip heat spreading

**On-chip heat spreading**
- Local ILVs, no TSVs
Monolithic 3D Integration (Wong, Mitra)

Application: PageRank (Google Datasets)

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Energy benefit</th>
<th>Delay benefit</th>
<th>Energy-Delay-Product benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>2D</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Monolithic 3D</td>
<td>25X</td>
<td>60X</td>
<td>1,500X</td>
</tr>
<tr>
<td>(CNFET, MRAM, RRAM)</td>
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</tbody>
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![Energy and Delay Comparison Diagram]

Imperfection-Immune Design Approach (Mitra, Wong)

1. CNT Computer
   - First Turing-complete CNFET processor

2. Co-optimized Processing & Design
   - Parameters
     - Pin/Pout
     - Sizing
     - CNT correlations

Mis-positioned CNTs

Imperfection-immune design & processing

- 1. Graph algorithms
- 2. Probabilistic analysis
- 3. Layout design

[Pi: Mitra, P. Wong, DAC ’13, Nature ’13, IEDM ’14]
Motivation:

- Si CMOS device performance increase commensurate with size scaling is beginning to saturate.
- Relentless scaling paradigm is also threatened by fundamental limits including power dissipation, communication bandwidth, and signal latency for both off-chip and on-chip interconnects.
- High efficiency solar cell technology is not economical

Objective

- Heterogeneous integration of alternate materials and structures for future ICs with scalability to future nodes
- Develop alternative technology for low cost high efficiency solar cells
Saraswat Group Research Projects

Nanoscale Ge & III-V MOSFET Technology
- Non-planar device structure for improved electrostatic integrity → low I_{off}
- Metal gate/high-k dielectric with improved scalability
- High mobility strained Ge or III-V channel → high I_{on}
- Integration on Si

Optical Interconnects
- Ge Optical Detector
- Optical Interconnects with Ge Laser

Capacitorless 1T-DRAM
- Junctionless Solar Cell
- Ge/Si Electro-Absorption Modulator

Synaptic Devices for Brain-Inspired Computing (Wong)
Brain-Inspired Computing (Wong)

Crossbar architecture inspired from grid-like connectivity of the brain

Pattern recognition on hardware using a 10x10 synaptic grid:

Phase change memory (PCM)

PCM array

PCM device

Synapses are implemented by PCM cells and neurons by software

S. B Eryilmaz, p 25.5 IEDM 2013.

Project Areas and Topics: X-on-Si and X-on-Flex

3D monolithic integration

X-on-Si

Integration of Atomically Thin 2D with 3D Materials and Devices (Pop)

Skin-like electrodes for long-term electrophysiological monitoring (Fan)

X-on-flex

Flexible electronic devices (Nishi)

autonomous sensors & energy

Mid- & near-field wireless power with stretchable electronics (Fan)

Chip-integrated Thermoelectric power for wireless sensor nodes (Fan)

Body Heat-Powered Autonomous Wearable Electronics (Pop)

Monolithic integration of AlGaN/GaN high electron mobility N/MEMS (Senesky)

Transfer Printing Methods for Integrating Thin Film Electronics onto Any Substrates (Zheng)

Heterogeneous integration of Ge and III-Vs on Si (Saraswat and Plummer)

Integration of Atomically Thin 2D with 3D Materials and Devices (Pop)

Skin-like electrodes for long-term electrophysiological monitoring (Fan)
Heterogeneous Integration on Si with Rapid Melt Growth (1)

- Deposited amorphous material contacts the Si substrate at a "seed hole"
- A microcrucible (Typically SiO₂) contains the target material
- The target material is melted in an RTA machine; crystallization occurs as it cools below the melting temperature
- Perfect single crystal material results suitable for device fabrication. The example chip shows a CMOS circuit with NMOS in the Si substrate and PMOS in recrystallized Ge

Heterogeneous Integration on Si with Rapid Melt Growth (2)

- Technique is applicable to binary compounds on Si
- Columns in blue have been recrystallized using RMG
Scaling Challenges of Transistors (Pop, Wong)

- **Challenge:** FETs "carved" out of bulk 3D materials (Si)  →  surface roughness restricts mobility, band gap, scaling of dimensions

- **Possible Solution:** FETs with atomically thin channel 1D and 2D materials (<1 nm) can re-enable $L_G$ scaling

Interfaces of Atomically Thin 2D Materials (Pop, Wong)

- **Today:** contact transfer lengths $L_T \sim 50$ nm

- **Goal:** scale down $L_T$ sub-10 nm by doping, edge injection and metal engineering
Flexible Electronics (J. Fan)

Fractal-based devices

- First iteration
- Second iteration
- Third iteration

Electromagnetic systems

- Multi-functional epidermal sensor
- Heating
- ECG and temp-measurement

Y. Nishi Group (with Y. Cui)

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Printed Electrochemical Transistors on Paper Substrates
Y. Nishi Group (with Y. Cui)

- Cellulose – most abundant polymer in the world
- Good mechanical properties, renewable, biodegradable

inkjet printed NWs

Printed Transistor on Cellulose Paper

inkjet printed P3HT or CNTs
**AlGaN/GaN High Electron Mobility M/NEMS (D. Senesky)**

- **Principal Investigator:**
  - Prof. Debbie G. Senesky
  - EXtreme Environment Microsystems Laboratory (XLab)

- **Research Summary:**
  - New breed of micro/nano-scale sensors and electronics for harsh environments
    - Temperatures > 600°C
    - Radiation
    - Chemically corrosive
  - Increase scientific knowledge of the physical mechanisms of electronic materials within unique environments

**Extreme Environment Gallium Nitride (GaN) Sensing Platform**

- Integration of Nanomaterials & Catalysts
- Radiation Exposure
- Integrated μCooling
- Wide Bandgap GaN HEMT Sensor
- High-Temperature Operation

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**Transfer Printing Methods for X-on-Flex (X. Zheng)**

- **Thin film electronics**
  - Transfer Printing
  - Rigid, Expensive Substrates
  - Flexible, Cheap Substrates

- **Wearable Memory Devices**

- **Cheap and Light Solar Cells**

- **Ultrathin Bio-sensors**

- **Attachable Electronics**
**Project Areas and Topics: Sensors and Energy**

- 3D monolithic integration
- AlGaN/GaN high electron mobility N/MEMS
- X-on-Si
- X-on-flex

### Autonomous Sensors & Energy

- Mid- & near-field wireless power with stretchable electronics (Fan)
- Chip-integrated thermoelectric power for wireless sensor networks (Gao et al.)
- Body-Heat-Powered Autonomous Wearable Electronics (Pop)
- Autonomous wireless sensor nodes for harsh environments via AlGaN/GaN heterostructures (Senesky)

### AlGaN/GaN Sensors (D. Senesky)

- Monolithic integration of AlGaN/GaN Embedded Sensors for Hot-spot Detection
- Electro-Thermal Hot Spot
- Sense Signatures for Control System

**SEM image of AlGaN/GaN high electron mobility strain sensors.**

**Metal-organic chemical vapor deposition system for GaN heterostructure growth.**
Energy Scavenging Sensors for Smart Buildings (Goodson)

- Smart Buildings bring multitudes of sensors and wiring.
- TE energy scavenging from heat sources (HVAC, water, windows) allows "truly wireless" sensor networks.
- Low power, low temperature TE conversion demands revolutionary new materials and design.

Thermoelectrics and “Self-Cooled” Electronics
E. Pop Group (with Goodson and Wong)

- Huge thermal anisotropy, good thermoelectric properties of nanomaterials
- Exploit thermal anisotropy for low-power electronics (e.g. phase-change memory)
- Separate thermal and electrical flow (thermal transistor, thermal diode)
- Electronics with built-in thermoelectric cooling
- Flexible thermoelectrics for energy harvesting from human body
HIEA Summary

- Moore-Like Scaling ~10x (??)
- Heterogeneous Integration ~10,000x

- Heterogeneous integration of:
  - Low power logic and memory
  - Sensors and energy harvesters
  - Novel nanomaterials

- Exploit heterostructures, thermal engineering, unconventional substrates